VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: C2 + TC2

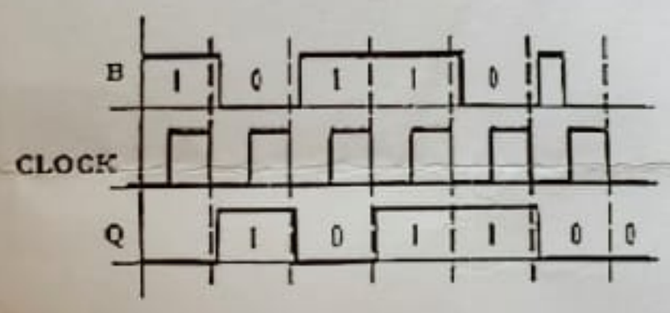
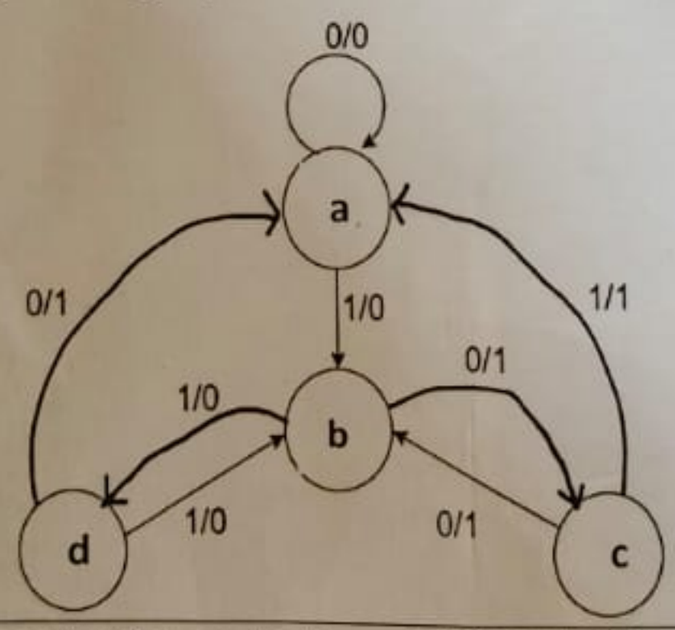
Room – 320

(10)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: M.Tech (Integrated) & Computer Science and Engineering**
Course Code and Course Name	**: IACSI202 - Digital Logic and Computer Design**
Faculty Name(s)	**: Ashutosh Mahajan, Mangaiyarkarasi R, Sathyanarayanan P**
Class Number(s)	**: VL2025260501083, VL2025260501087, VL2025260501085**
Date of Examination	**: 17/03/2026**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s): Answer All Questions

Q. No	Question	Marks
1. ✓	Implement the following Boolean function F(A, B, C, D) =∑m (0,1,4,6,7,9,11,15) using only one 4×1 Mux and external gates. Consider AB as select lines.	10
2.	Design a 2-bit magnitude comparator for the binary number $X= X_1X_0$ and $Y=Y_1Y_0$. The outputs A, B and C, Where A is 1 if X > Y, B is 1 if X = Y and C is 1 if X < Y. Implement the comparator using two 3-to-8-line decoder.	10
3.	An XY Flipflop is designed with two inputs, X (set) and Y (reset), and a clock pulse. The Flipflop operates as follows: "On the rising edge of the clock, the output Q becomes 1 if X=1 and Y=0. If X=0 and Y=1, Q becomes 0. If both the inputs are 0, the state is held and if both inputs are 1, the output toggles. Identify the XY Flipflop and convert it to B flipflop. Refer the timing diagram of the B Flipflop shown below (Fig 1).  Fig1: Timing of B Flipflop	10
4.	The given state diagram below has one input and one output. Obtain the state table and design the sequential circuit using a JK Flipflop? Consider the states a-00, b-11, c-10, and d-01, respectively. 	10
5.	Create a synchronous counter that cycles through 0-3-5-4-1-0 using D Flipflop	10