VIT
Vellore Institute of Technology

REG.NO.:

SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

SLOT:B1+TB1

Programme Name & Branch	: B.Tech [IT]
Course Code and Course Name	: BAITE101 and Digital Logic Design and Computer Organization
Faculty Name(s)	: Dr.K.Santhi, Dr. M.Pradeepa, Dr. P.Suganya
Class Number(s)	: VL2025260105834, 7927, 5838
Date of Examination	: 18-08-2025
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

CO1: Outline the conversion of number systems and illustrate the simplification of Boolean functions and design combinational circuits

CO2: Construct the design and analysis of various Sequential logic circuits using flip

Q. No	Question	M	CO	BL
1.	a) Convert 132478.235_{10} to Octal and Hexadecimal number system.	4	1	1
	b) Simplify the following Boolean function $F(A, B, C, D) = \sum_m(0,1,4,5,6,7,9,11,14,15)$ and implement it using NAND gates	6		
2.	Define 4 variable (w,x,y and z) scenario as given below • w=1 if the applicant has been involved in a car accident • x = 1 if applicant is married • y =1 if applicant is male • z =1 if the applicant is under 25 Find the Boolean expression which assumes the value 1 when the policy should be issued: a. A Married female 25 years old or over b. A female under 25 c. A married male under 25 who has not been involved in a car accident d. A Married male who has been involved in a car accident e. A married male 25 years old or over who has not been involved in a car accident. Reduce the Boolean expression using K-Map.	10	1	2
3.	Refer to Figure below, where an analog-to-digital converter is monitoring the dc voltage (VB) of a 12-V storage battery on an orbiting spaceship. The converter's output is a four-bit binary number, ABCD, corresponding to the battery voltage in steps of 1 V, with A as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is greater than 0110; that is, the battery voltage is greater	10	1	3

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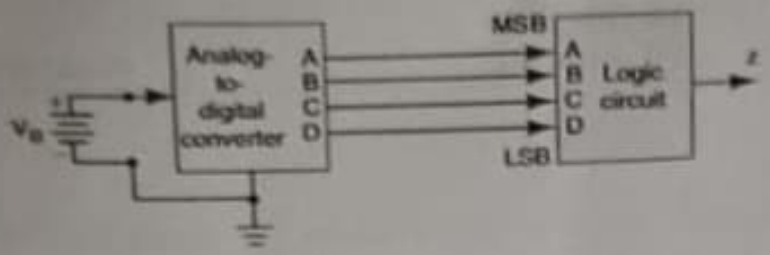
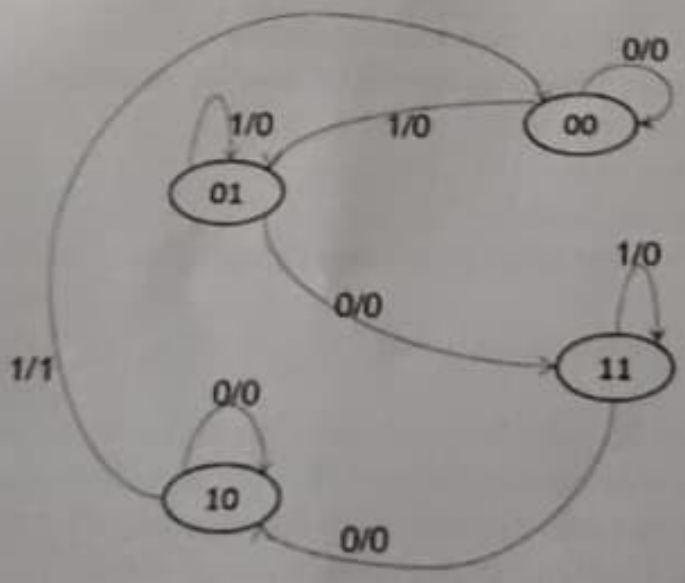
	than 6 V. Identify the Boolean function and design this logic circuit using 4*1 multiplexer. 		
4.	A XY flip flop has four operations. When inputs X and Y are 00, 01, 10 and 11, the outputs are Toggle, 1, 0 and No change respectively. If you have a flip flop as specified above, then i) Tabulate the characteristic table. ii) Derive the characteristic equation iii) Draw the state diagram iv) Derive the Excitation table.	10	2
5.	Find the state table and design a synchronous sequential circuit using T flip flop for the following state diagram shown below. 	10	2