(Deemed to be University under section 3 of UGC Act, 1956)

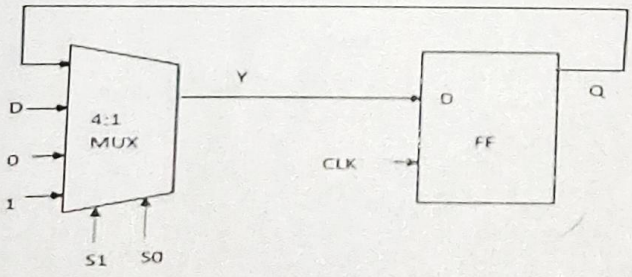
SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - 2
WINTER SEMESTER 2025-2026

SLOT: G1+TG1

Programme Name & Branch	**:B.Tech &ECE/BML**
Course Code and Course Name	**: BAECE102-Digital Logic Design**
Faculty Name(s)	**:Dr Ravi S, Dr Rajeshkumar V, Dr. Hemanta Kumar Sahu, Dr Deepikarani Sona, Dr. Abhishek Narayan Tripathi**
Class Number(s)	**: VL2025260500805, 0807, 0810, 0812, 0814**
Date of Examination	**:23/03/2026**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- Course Outcomes
  CO2 : Implement the various combinational and sequential circuits for customized specification
  CO3: Use the Verilog HDL constructs to model all the combinational and sequential logic circuits

Q. No	Question	M	CO	BL
1.	Design a 4-to-2 priority encoder with inputs I_0, I_1, I_2, I_3 where I_1 has the highest priority and I_3 has the lowest priority. ($I_1 > I_2 > I_0 > I_3$). (a) Construct the truth table considering priority conditions. (b) Derive the Boolean expressions for outputs Y_1 and Y_0 . (c) Implement the circuit using basic logic gates.	10	2	3
2.	Design and implement a circuit using a 4×1 Multiplexer with three inputs (A, B, C) and one output (Y). The output Y = 1 when the number of 1's in the input is even, otherwise Y = 0. Construct the truth table. Connect A and C inputs to the select line. Determine the required MUX input connections (I_0–I_3). Draw the MUX implementation diagram.	10	2	3
3.	A new clocked X-Y flip-flop is defined with two inputs, X and Y. The flip-flop functions as follows: If X is not equal to Y, the flip-flop remains unchanged in its state (Q) at the next clock pulse, and if X is equal to Y, the flip-flop toggles its state (Q) at the next clock pulse. (a) Provide the truth table for the X-Y flip-flop. (b) Provide the characteristics table. (c) Provide the Excitation table for the X-Y flip-flop. (d) Implement the X-Y flip-flop using a J-K flip-flop.	10	2	3
4.	Design a synchronous counter for the count sequence 0-2-5-7-3-1-0 using a positive-edge-triggered D flip-flop.	10	2	3
5	Write the Behavioral Verilog code and test-bench describing the functionality of the circuit given in Figure 1.  Figure-1	10	3	3