VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

SLOT: F2+TF2

Programme Name & Branch	: BTech ECE/CSE
Course Code and Course Name	: BECE102L & Digital System Design
Faculty Name(s)	: NITHISH KUMAR V, SUMIT KUMAR JINDAL, HEMALATHA K, ARUN DEV DHAR DWIVEDI, AVINASH CHANDRA RAGUNATH G, ASHUTOSH MAHAJAN, NAVEEN MISHRA, JAFFINO, HANIDUL HOQUE MOHIUL ISLAM, LAVANYA N, RAJA SELLAPPAN, HEMANTA KUMAR SAHU KALYANBRATA GHOSH, VIVEK RAJPOOT, SAURABH NAGAR, SHILPI RUCHI KERKETTA SUKANTA KUMAR TULO, ABHISHEK NARAYAN TRIPATHI, DILIP KUMAR CHOUDHARY RAJKISHOR KUMAR, MANISH KUMAR, HENRIDASS, BIJAYLAXMI DAS
Class Number(s)	: VL2025260102576, 3579, 3581, 3584, 3586, 3588, 3590, 3592, 3597, 3599, 3602, 3604, 3606, 3609, 3612, 3614, 3618, 3620, 3623, 3628, 3629, 3637, 3642, 3648, 3653
Date of Examination	: 22.08.25
Exam Duration	: 90 minutes (2.00 PM – 03.30 PM)

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes are:

C01: Optimize the logic functions using and Boolean principles and K-map.
C02: Model the Combinational and Sequential logic circuits using Verilog HDL.
C03: Design the various combinational logic circuits and data path circuits.

S.No.	Question	CO	BL	Marks
1.	Use Boolean law/postulates to derive the minimized expression for the following a) Y = AB+ (AC)'+AB'C (AB+C) b)Y = (A'B'C'D'+A'B'C'D+A'B'CD+A'BC'D+ A'BCD+ A'BCD' +AB'CD'+ABC'D+ABCD'+ABCD)	1	BL3	5+5
2.	Apply the K-Map on the Boolean function F (W,X,Y,Z) = Σm (0,7,8,9,10,12) + d (2,5,13) to obtain the minimized SOP and POS and also draw the logic diagram for the minimized POS with NAND gates only.	1	BL3	10
3.	a) Identify the errors in the verilog program given:	2	BL2	5+5

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	Module 2bitmc(a,b,equal, greater, lower);
	output equal, greater, lower;
	input [1;0]a,b;
	net wo,w1,w2,w3,w4,w5;
	xnor(w0,a[0],b[0]);
	xnor(w1,a[0],b[1]);
	not(b1[0],b[0]);
	not(b1[1],b[1]);
	and(w5,a1[0],b[0],w0);
	or(w2,w3,greater);
	or(lower, w4,w5)
	and(equal,w0,w1);
	end module;
	
	b) Recognize the output of the each operation in the verilog code.
	i. Y1 = {2{3'b110,2{2'b1x}}}
	ii. Y2= -11%3
	iii. Y3= 8'b10011011<<3
	iv. Y4 = (4'b101z = = =4'b110z)
	v. Y5 = (3'b101 && 4'b1010)			

4.	Develop a gate level modeling for the data flow code shown below.
	
	module my_ckt (w, x, y, z, a, b, c, d);
	input w, x, y, z;
	output a,b,c,d;
	assign a = ((w & x) | (w & y & z));
	assign b = (((~x) & (~y)) | ((~x) & (~z)) | (x & y & z));
	assign c = (((~y) & z) | (y & (~z)));
	assign d = ~z;
	endmodule
		2	BL3	10

5.	Construct a combinational circuit to automate the packaging of balls in the industry. The items will be packed based on the following scenarios: a) if two or three balls are available in the box, then the package will be done i.e., output is HIGH. (b) If none or one ball is available in the box, then the package will not be done i.e., output is LOW. Note : Consider output as don't care if more than three ball are available in the box.	3	BL3	10