Vellore Institute of Technology

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

SLOT: G2+TG2

Programme Name & Branch	: B.Tech ECE
Course Code and Course Name	: BECE102L & Digital System Design
Faculty Name(s)	: ARUNACHALAM V, PALLA PENCHALAIAH, VETRIVEERAN RAJAMANI, VISHAL GUPTA, DEBASHISH DASH, DHANABAL R
Class Number(s)	: VL2025260100493, 0495, 0498, 0501, 2551 & 2560
Date of Examination	: 23.08.25
Exam Duration	: 90 minutes (2.00 PM – 3.30 PM)

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level
  (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes are:
C01: Optimize the logic functions using and Boolean principles and K-map.
C02: Model the Combinational and Sequential logic circuits using Verilog HDL.
C03: Design the various combinational logic circuits and data path circuits.

S.No.	Question	CO	BL	Marks
1.	a) Use Boolean law/postulates to derive the minimized expression for the function $F = (A + (BC)')'(AB' + ABC)$ and mention the number of NOR gates required for the minimized expression to realize it. b) For a Boolean function F(A,B) = Σm(0,2), prove that F(A,B) = Π M(1,3) and F' (A,B) = Σ m(1,3) = ΠM(0,2)	1	BL3	5+5
2.	Apply the K-Map on the Boolean function $F(A,B,C,D) = \Sigma m(0,1,2,5,7,8) + \Sigma d(3,6,10)$ to obtain the minimized SOP and POS and also draw the logic diagram for the minimized SOP with NOR gates only.	1	BL3	10

3.	a) Identify the errors in the verilog program given below:
	module half adder(a, b, sum, carry);
	input a b;
	output reg sum, carry;
	wire temp_sum, temp_carry;
	assign temp_sum = a ^ b;
	assign temp_carry = a & b;
		2	BL2	5+5

REG.NO.:

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	sum = temp_sum;
	carry = temp_carry
	endmodule;
	b) Recognize the output of the each assignments in the verilog code with the given input A = 4'b10xz; B = 4'b10x1; C = 3'b01x; D = 3'b01z;
	i. Y1= (C === D)
	ii. Y2= { 2{A[3:2]}, B[3:1], 1'bZ, A[0] }
	iii. Y3= A | B
	iv. Y4=(A == B) && (|B)
	v. Y5= ~(A & B);			

4.	Develop a verilog code in gate-level modeling for a combinational circuit which has three inputs and one output. The output is '1' if only two inputs are high, otherwise '0'.	2	BL3	10
5.	Construct the combinational circuit for the lighting of an office building with three sensor inputs and three light outputs to automate the lighting system based on sensors. An individual office light (X) should be turned-on if motion (A) ('1' for movement detected, '0' for no movement) has been detected in the office. Hallway lights (Y) should be turned-on if any office lights on that hallway have been on, or any motion in the hallway detected (B). Staircase lights (Z) should be on if any office lights and hallways have been on, or any motion in the staircase detected (C). Draw the logical diagram of the circuit with NAND gates only.	3	BL3	10