



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 24BCT0276

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: F2+TF2

Programme Name & Branch : B.Tech – BEC, BCT, BCB, BCI, BDS, BKT, BML, BCE
 Course Code and Course Name : BECE102L & Digital System Design
 Faculty Name(s) : NITHISH KUMAR V, SUMIT KUMAR JINDAL, HEMALATHA K, ARUN DEV DHAR DWIVEDI, AVINASH CHANDRA RAGUNATH G, ASHUTOSH MAHAJAN, NAVEEN MISHRA, JAFFINO, HANIDUL HOQUE MOHIUL ISLAM, LAVANYA N, RAJA SELLAPPAN, HEMANTA KUMAR SAHU KALYANBRATA GHOSH, VIVEK RAJPOOT, SAURABH NAGAR, SHILPI RUCHI KERKETTA SUKANTA KUMAR TULO, ABHISHEK NARAYAN TRIPATHI, DILIP KUMAR CHOUDHARY RAJKISHOR KUMAR, MANISH KUMAR, HENRIDASS, BIJAYLAXMI DAS
 Class Number(s) : VL2025260102576, 3579, 3581, 3584, 3586, 3588, 3590, 3592, 3597, 3599, 3602, 3604, 3606, 3609, 3612, 3614, 3618, 3620, 3623, 3628, 3629, 3637, 3642, 3648, 3653
 Date of Examination : 10.10.25
 Exam Duration : 90 minutes (9.30 AM – 11.00 AM) Maximum Marks: 50

General instruction(s): Answer All Questions

- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes :
 CO2: Model the Combinational and Sequential logic circuits using Verilog HDL.
 CO3: Design the various combinational logic circuits and data path circuits.
 CO4: Analyze and apply the design aspects of sequential logic circuits.

Q. No	Question	M	CO	BL
1.	Design the given Boolean expression $Y = a \oplus b \oplus c$ using a 4 x 1 multiplexer with "a" and "c" as the select lines and write the behavioural verilog program for the design.	10	2	3
2.	Using a 2 x 4 decoders and external gates, design the combinational circuit defined by the following three Boolean functions: $F1 = x'y'z + xz'$ $F2 = x'yz' + xy'$ $F3 = xyz' + xy$	10	3	3
3.	Construct the logical diagram for a 4 to 2 priority encoder, has the priority order as $D1 > D0 > D2 > D3$ ($D1$ is the highest priority and $D3$ is the least priority).	10	3	3



VIT[®]

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: F2+TF2

4.	Show the steps involved in multiplying +5 with -7 using a 5-bit Booth's multiplier. Determine the final product and the number of addition and subtraction operations performed.	10	3	3																														
5.	Realize the X flip-flop using Y flip-flop. The characteristic table of X and Y flip-flops are as follows <table border="1" data-bbox="506 826 970 1184" style="display: inline-table; margin-right: 20px;"> <thead> <tr><th>X</th><th>Q(t)</th><th>Q(t+1)</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> <table border="1" data-bbox="1102 826 1566 1184" style="display: inline-table;"> <thead> <tr><th>Y</th><th>Q(t)</th><th>Q(t+1)</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Q(t)	Q(t+1)	0	0	0	0	1	0	1	0	1	1	1	0	Y	Q(t)	Q(t+1)	0	0	1	0	1	1	1	0	0	1	1	0	10	4	3
X	Q(t)	Q(t+1)																																
0	0	0																																
0	1	0																																
1	0	1																																
1	1	0																																
Y	Q(t)	Q(t+1)																																
0	0	1																																
0	1	1																																
1	0	0																																
1	1	0																																
