VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: G2+TG2

B.Tech ECE - BECE102L & Digital System Design - Maximum Marks: 50

Key for Evaluation

S.No.	Question	Marks
1.	Design a three-input majority circuit, whose output is 'HIGH' if the input has more 1's than 0's, otherwise 'LOW', using 2-to-4 decoders. Write the behavioural Verilog code for the design.	10

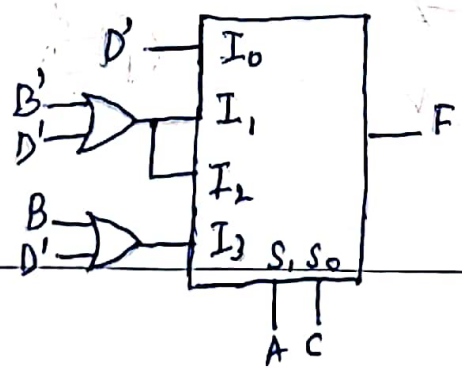
```
module decoder(input enable, input [1:0] in,
output reg [3:0] out);
 always @(*) begin
   out = 4'b0000;
   if (enable) begin
     case (in)
       2'b00: out = 4'b0001;
       2'b01: out = 4'b0010;
       2'b10: out = 4'b0100;
       2'b11: out = 4'b1000;
       default: out = 4'b0000;
     endcase
   end
 end
endmodule
```

```
module func (input A,B,C, output reg y);
wire [3:0] O1, O2;
decoder d1( (~A), ({B,C}), O1);
decoder d2( (A), ({B,C}), O2);
always @(*) begin
  y<=(O1[3]|O2[1]|O2[2]|O2[3]);
  end
endmodule
```

S.No.	Question	Marks
2.	Using a 4×1 multiplexer design, the combinational circuit has four inputs (A, B, C, D), whose output is '1' if the input is divisible by 2 or 3, otherwise '0'. The inputs A and C are connected to the select lines of the multiplexer.	10

Possible minterms are 0 to 15;
{0,2,4,6,8,10,12,14} are divisible by 2;
{0,3,6,9,12,15} are divisible by 3;
Therefore, F(A,B,C,D) = ∑(0,2,3,4,6,8,9,10,12,14,15)

AC	*I0*	*I1*	*I2*	*I3*
	00	*01*	*10*	*11*
B'D'	*1 (0)*	*1 (2)*	*1 (8)*	*1 (10)*
B'D	*(1)*	*1 (3)*	*1 (9)*	*(11)*
BD'	*1 (4)*	*1 (6)*	*1 (12)*	*1 (14)*
BD	*(5)*	*(7)*	*(13)*	*1 (15)*
	I0=B D'+B'D' =D'	*I1=B' D'+B'D+BD' =B'+D'*	*I2=B'+D'*	*I3=B' D'+BD'+BD =B+D'*



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3. A hospital's emergency room uses a priority encoder to decide which gate to open and which patient should be treated next. The encoder takes 4 input lines corresponding to 4 levels of emergency: (10)

D1 Cardiac Arrest (Highest)
D2 Major Injury
D0 Moderate Illness
D3 Minor Issue (Lowest)

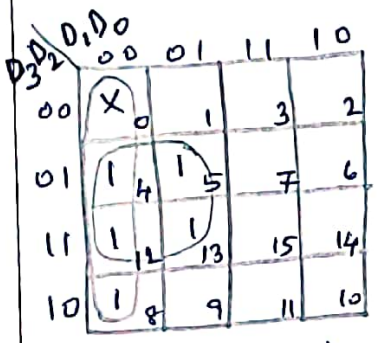
Design a logic circuit for the above.

D3	D2	D1	D0	O1	O0	V
0	0	0	0	X	X	0
X	X	1	X	0	1	1
X	1	0	X	1	0	1
X	0	0	1	0	0	1
1	0	0	0	1	1	1

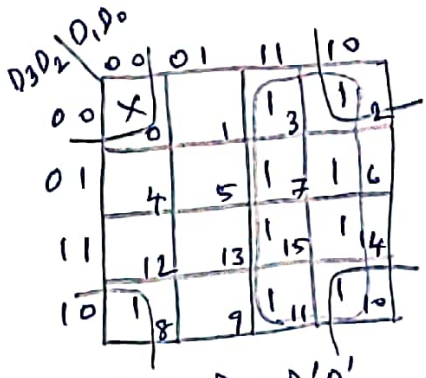
$O1 = \sum m(4,5,8,12,13) + \sum d(0)$

$O0 = \sum m(2,3,6,7,8,10,11,14,15) + \sum d(0)$

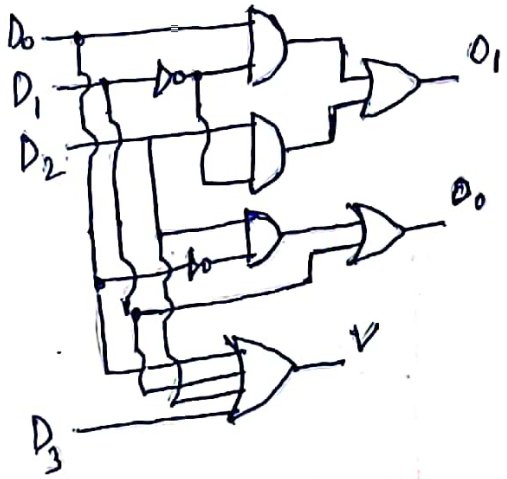
$V = D3+D2+D1+D0$



$O1 = D_2 D_1' + D_1' D_0$



$O0 = D_1 + D_2' D_0'$



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4. Detail the steps involved in multiplying (-10) by (-7) using the Booth algorithm and estimate the number of additions and subtractions required. **10**

A	Q	Q_{-1}	M	C	Remarks
00000	11001	0	10110	5	M = 2's (01010) = 11001; Q = 2's (00111) = 11001;
01010 00101	11001 01100	0 1	10110	4	(10), $A \leftarrow A - M$; A = 00000 + 01010 = 01010; Shift right (Arithmetic)
11011 11101	01100 10110	1 0	10110	3	(01), $A \leftarrow A + M$; A = 00101 +10110 = 11011; Shift right (Arithmetic)
11110	11011	0	10110	2	(00), Shift right (Arithmetic)
01000 00100	11011 01101	1 1	10110	1	(10), $A \leftarrow A - M$; A = 11110 + 01010 = 01000; Shift right (Arithmetic)
00010	00110	1	10110	0	(11), Shift right (Arithmetic)

The number of additions and subtractions required is 3.
$(-10)\times(-70) = 70$; 1000110 is $2^6 + 2^2 + 2^1 = 64 + 4 + 2 = 70$

5. A customised (AB) flip-flop has the following characteristics. **10**

A	B	(Q_{n+1})
0	0	1
0	1	Q_n
1	0	Q_n
1	1	0

a) Provide the excitation table for the AB flip-flop.
b) Realise a J-K flip-flop using an AB flip-flop.

(a) Excitation table

Q_n	Q_{n+1}	A	B
0	0	X	1
0	1	X	0
1	0	1	X
1	1	0	X

(b) Implementation table

J	K	Q_n	Q_{n+1}	A	B
0	0	0	0	X	1
0	0	1	1	0	X
0	1	0	0	X	1
0	1	1	0	1	X
1	0	0	1	X	0
1	0	1	1	0	X
1	1	0	1	X	0
1	1	1	0	1	X