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VIT®

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
MID-TERM EXAM
WINTER WEI SEMESTER 2024-2025

SLOT:X11+X12+X21

Programme Name & Branch	**: B.Tech, Computer Science, Electronics & Communication**
Course Code and Course Name	**: BECE102L & Digital Systems Design**
Faculty Name(s)	**: DEBASHISH DASH**
Class Number(s)	**: VL2024250507402**
Date of Examination	**: 08th March 2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  1. Optimize the logic functions using and Boolean principles and K-map.
  2. Model the Combinational and Sequential logic circuits using Verilog HDL.
  3. Design the various combinational logic circuits and data path circuits.
  4. Analyze and apply the design aspects of sequential logic circuits.
  5. Analyze and apply the design aspects of Finite state machines.
  6. Examine the basic architectures of programmable logic devices.

Q. No	Question	M	CO	BL
1.	Simplify the following Boolean expression which represents the output of a logical decision circuit. $f(A,B,C,D,E) = (AB + C + D)(\bar{C} + D)(\bar{C} + D + E)$	10	1	3
2.	Neatly draw a basic full adder and write verilog HDL for it using structural design method.	10	2	4
3.	a) Implement a 2 to 4 binary decoder along with its truth table, logic expressions and logic diagram using basic gates.	5	3	3
	b) Implement a 4 to 2 binary encoder along with its truth table, logic expressions and logic diagram using basic gates.	5		
4.	a) What are the abstraction levels associated with Verilog HDL? Briefly describe regarding them.	5	2	2
	b) Briefly describe regarding the Verilog modelling design flow to create a suitable electronics product.	5		
5.	Minimize the given Boolean function using K-map. Implement the minimized function only using AOI gates. $f(A,B,C,D) = \sum(3,4,5,7,9,13,14,15) + d(0,2,8)$	10	1	3

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