REG.NO.:

SLOT: D1

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

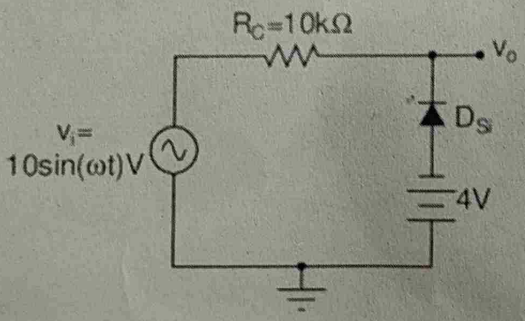
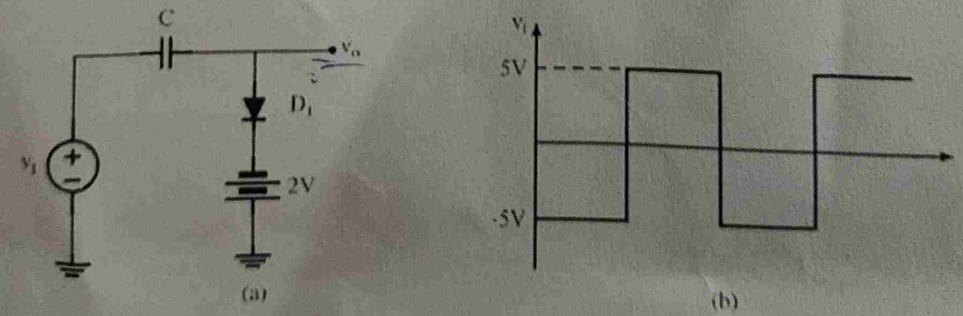
SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

Programme Name & Branch : B.Tech & BEE, BEI
Course Code and Course Name : BEEE205L & Electronic Devices and Circuits
Faculty Name(s) : Sankardoss V, Chilukuri Venkata Mahendra, Uma Sathyakam P
Class Number(s) : VL2025260101210, VL2025260101215, VL2025260101214
Date of Examination : 20/08/2025
Exam Duration : 90 minutes
Maximum Marks: 50

General instruction(s):

- Answer All Questions
- Rough work should not be done on question paper. It will be treated as malpractice.
- Use ordinary graph sheet.
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes Statements:
CO. 1: Solve diode circuits for various applications.
CO. 2: Analyze and design BJT and MOSFET DC circuits and their amplifier configurations.

Q. No	Question	M	CO	BL
1a.	Sketch the input and output waveform of the clipper circuit shown in Fig. 1 on a graph sheet, when an input of 1 kHz sinewave is applied assuming ideal diodes. Describe the operation briefly.  Fig. 1	5	1	3
1b.	Fig. 2 (a) shows the clamper circuit and the corresponding input waveform in Fig 2(b). Obtain the steady state output waveform and draw it on a graph sheet.  Fig. 2	5	1	3

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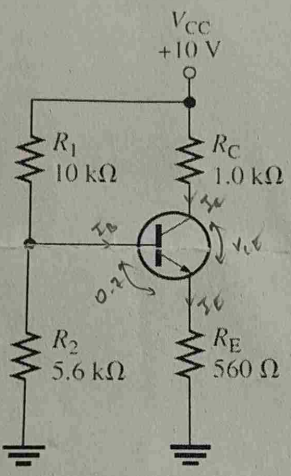
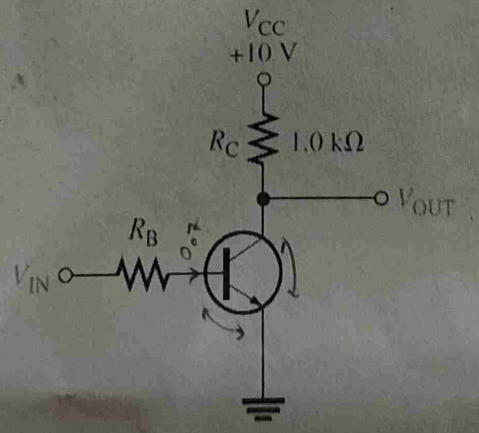
2.	A crystal diode having internal resistance r_f = 20 Ω is used for half-wave rectification. If the applied voltage v = 50sinωt and load resistance R_L = 800 Ω, Find: (a) I_m, I_{dc}, I_{rms}, (b) a.c. power input and d. c. power output, (c) d. c. output voltage and (d) efficiency of rectification	10	1	2
3.	With neat diagram, explain the input and output characteristics of a NPN transistor in CE configuration and draw it on a graph sheet.	10	2	1
4.	Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of Fig. 3 if β_{DC} = 100.  Fig. 3	10	2	3
5.	(a) For the transistor circuit shown in Fig. 4, what is V_{CE} when V_{IN} = 0 V? (b) What minimum value of I_B is required to saturate this transistor if β_{DC} is 200? Neglect $V_{CE(sat)}$. (c) Calculate the maximum value of R_B that will put the transistor in saturation assuming β_{DC} = 200 when V_{IN} = 5 V.  Fig. 4	10	2	3