VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 23BEC0309

SCHOOL OF ELECTRONICS ENGINERRING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

SLOT: G1

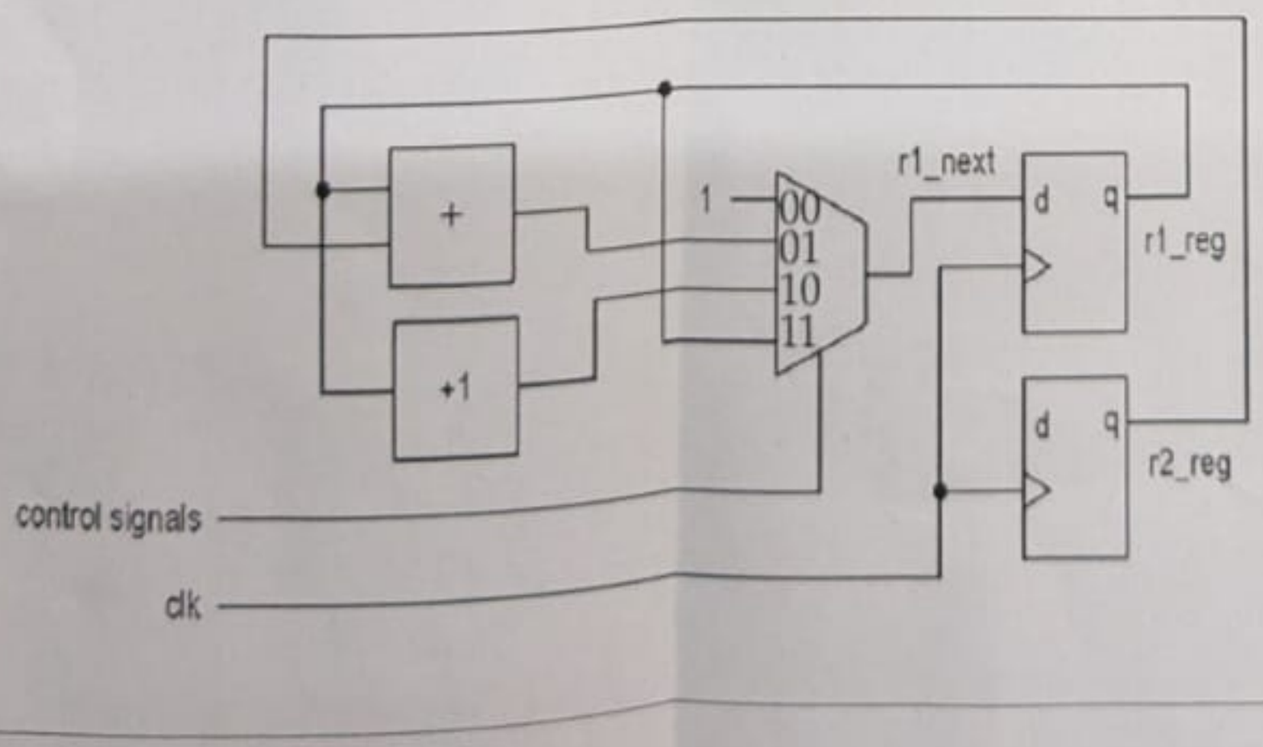
Programme Name & Branch	: B.Tech - ECE
Course Code and Course Name	: BECE406E – FPGA Based System Design
Faculty Name(s)	: Prof. Aarthy M
Class Number(s)	: VL2025260500872
Date of Examination	: 02.02.26
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

1. Understand architectures of programmable logic devices
2. Understand various abstraction level in Verilog HDL
3. Construct high speed arithmetic and memory circuits

Q. No	Question	M	CO	BL
1.	Briefly discuss about the IC Classification based on Programmability. Draw and explain the architecture of ALTERA MAX CPLD	10	1	2
2.	Implement the below logic functions i) F1(x,y,z) = (xy +z) (y+xz) using PROM ii)F2(x,y,z) = (x+y) (x'+y+z) (x'+y+z') using PAL	10	1	3
3.	Design the below circuit using structural modelling in Verilog HDL. Control signals, clk and rst are the inputs and r1_reg and r2_reg are the outputs of the circuit. Model the DFF with synchronous reset using behavioural modelling and 4x1 Mux using dataflow modelling. Assume the adder and incrementer modules are available. 	10	2	3

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4.	Briefly discuss and compare the various high-speed adders. Also, provide a schematic diagram and explain 16-bit carry-select adder using 4-bit ripple carry adders (RCA)/carry-lookahead adders (CLA).	10	3	2
5.	(a) Design an array multiplier using full adders to perform F = X * Y where X and Y are 3 bits with proper schematic diagram. [3 Marks] (b) Write the Verilog code using structural modelling for the 3-bit multiplier designed in Q.5 (a). [3 Marks] (c) Explain the steps involved in the multiplication of 4 x 6 using shift right and add algorithm. How many iterations/clock cycles are required to generate the product? [4 Marks]	10	3	3

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