Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

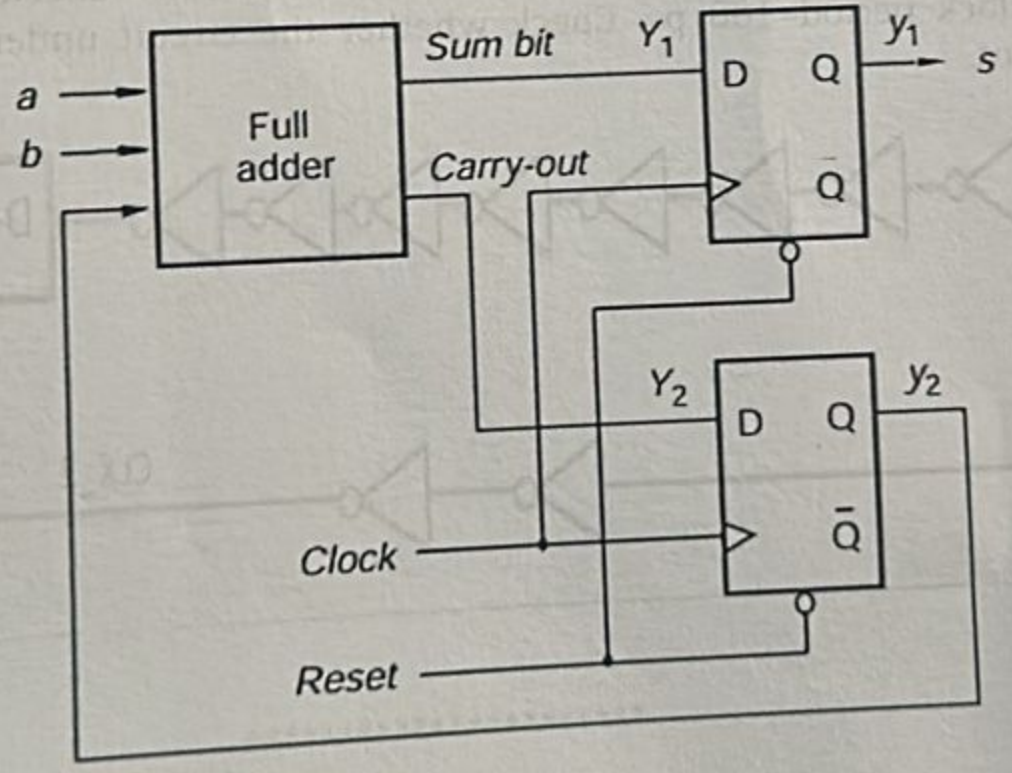
SCHOOL OF ELECTRONICS ENGINERRING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

SLOT: G2

Programme Name & Branch : B.Tech - ECE
Course Code and Course Name : BECE406E – FPGA Based System Design
Faculty Name(s) : Prof. Aarthy M
Class Number(s) : VL2025260500873
Date of Examination : 23.03.26
Exam Duration : 90 minutes
Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Q. No	Question	M	CO	BL
1.	Design a sequence detector circuit that has IN, RESET and CLK as the inputs and OUT as the output. The output OUT will be 1 when the input sequence 1011 are the last 4 inputs received on IN otherwise the output OUT will be 0. The detector should keep checking for the appropriate sequence and should not reset to the initial state after it has recognized the sequence. The detector initializes to a reset state when input, RESET is activated. Also, make sure the output OUT of the circuit is dependent on the input and present state of the circuit. Implement the sequence detector using behavioural modelling style in Verilog HDL.	10	3	3
2.	Analyse the circuit given below and explain the functionality of the circuit using the state transition diagram. Implement the design using behavioural modelling style in Verilog HDL. 	10	3	3

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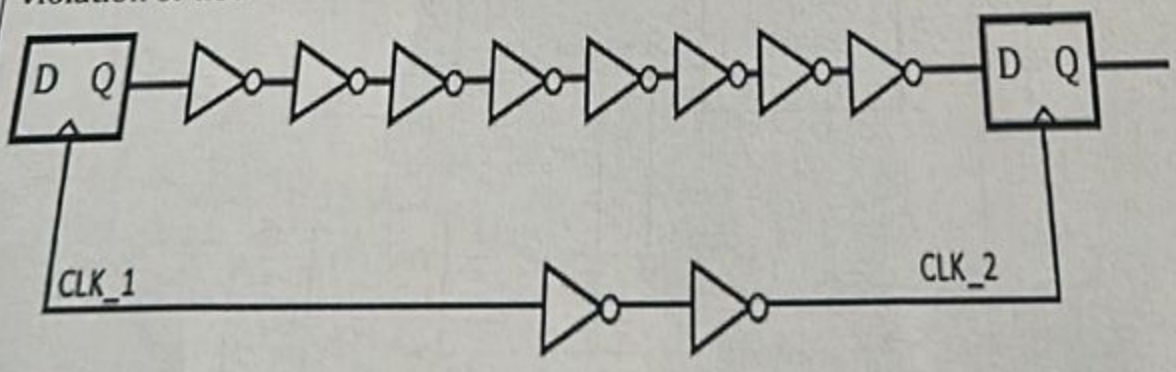
3.	A synchronous FIFO is used for buffering data between modules operating with the same clock. a) Explain how overflow and underflow conditions occur and how they are prevented. b) Design a FIFO of depth 16 and data width 8 bits using Verilog. c) Write a testbench to verify FIFO functionality and generate test cases to check overflow and underflow conditions.	10	3	2
4.	Two modules, A and B, in a processor communicate through a FIFO buffer. Based on the given parameters, determine the minimum FIFO depth required in each case. (a) Module A writes data to the FIFO at 200 MHz, while module B reads data at 50 MHz. The burst size is 120 words. The duty cycle of the write enable signal is 50%, and the duty cycle of the read enable signal is 25%. Calculate the minimum FIFO depth required. (b) Module A writes data at 40 MHz, and module B reads data at 80 MHz. The burst size is 100 words, and there is no idle cycle between the read and write operation. Determine the minimum FIFO depth required. (c) Both write and read operations occur at 50 MHz for module A, B. The burst size is 100 words, and there is no idle cycle between the read and write operation. Calculate the minimum FIFO depth required.	10	4	2
5.	The circuit given below has eight inverters between the two flops. Assume, each inverter has a delay of 25ps, and the flops have t_{su} = 12.5ps and $t_{clk\text{-}to\text{-}Q}$=37.5ps. What is the maximum operating frequency of this circuit? Check the setup violation if clock period=100 ps. Check whether the circuit undergoes hold violation or not. 	10	4	3

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