Y/K/TY

Reg. No: [redacted]

Final Assessment Test – November 2025

VIT® Vellore Institute of Technology (Deemed to be University under section 3 of the UGC Act, 1956)

Course: **BACSE103 - Computation Structures**

Class NBR(s): **7232/7234/7238/7240/7241/7244/7245/7249/7251/7253/7302/7304/7306/7311**

Slot: **D1+TD1**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	To design and optimize minimal combinational circuits.
CO2	To analyze and design sequential circuits utilizing various types of flip-flops.
CO3	To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations
CO4	To understand the concept of memory organization and I/O fundamentals
CO5	To understand the microcontroller architectural designs and parallel computing systems

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. A digital design engineer is tasked with designing a fast 4-bit adder for a microprocessor. The engineer notices that the conventional ripple carry adder introduces significant delay because each bit's carry must wait for the previous carry. The inputs to the 4-bit numbers are: **CO1 BL3**

$$A = 1011_2, B = 1101_2$$

   i. Explain why the ripple carry adder suffers from carry propagation delay. **[2]**

   ii. Using the Carry Look-Ahead Adder (CLA) principle, compute the carry signals C_1, C_2, C_3, C_4. **[4]**

   iii. Determine the sum bits for the addition using CLA. **[2]**

   iv. Discuss the advantage of using a CLA over a ripple-carry adder in this scenario. **[2]**

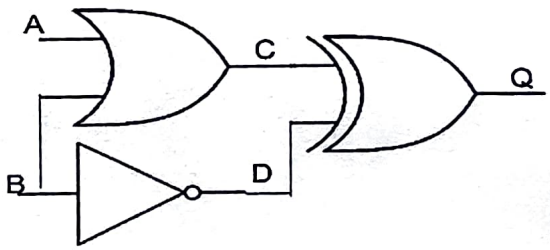
2. Design a MOD-4 synchronous up-counter, using JK flip flop. **CO2 BL3**

3. Describe Booth's multiplication algorithm and demonstrate its step by multiplying -12 × 11. **CO3 BL3**

4. Develop an assembly-level program that converts Celsius temperature to Fahrenheit (F=9/5*C+32) utilizing a one-address instruction format and explain each instruction. **CO3 BL3**

5. Design a 1024 x 8 bit using 256 x 8 bit RAM chips. **CO4 BL3**

6.	Explain how associativity affects the choice of cache replacement algorithm. Given a cache of 3 blocks and a memory access sequence: 7, 0, 1, 2, 0, 3, 0, 4, 3, 5, 4, 5, 3, 0, 2 compute the number of cache hits and misses using: i) FIFO ii) LRU	CO4	BL3
7.	Explain how the stack is used during subroutine calls and returns in an ARM processor. Describe the role of the linkage register and program counter in the process.	CO5	BL2
8.	Explain Instruction-Level Parallelism (ILP) in modern processors. Discuss its key features, benefits, and applications.	CO5	BL2
9.a)	i. Construct an 8 to 1 multiplexer using 2 to 1 multiplexers. Justify the working of the circuit by explaining what happens when the select lines are S_2=1, S_1 = 0, S_0 = 1. Identify which input gets selected and explain the data flow.	CO1	BL3
	ii. State the difference between a multiplexer and a decoder.		
	OR		
9.b)	i. Reduce the given function F(A,B,C,D) = Σ (1,2,3,5,8,10,11,12) using kmap.	CO1	BL3
	ii. For the logic circuit below construct the truth table.		



10.a)	Describe the working principle of an SR flip-flop with a neat diagram and truth table.	CO2	BL2
	OR		
10.b)	Describe the working principle of an JK flip-flop with a neat diagram and truth table.	CO2	BL2

⇔⇔⇔ **Y/K/TY** ⇔⇔⇔