A/L/TY

Reg. No:

VIT
Vellore Institute of Technology

# Final Assessment Test - November 2025

Course: BACSE103 - Computation Structures

Class NBR(s): 5815 / 5817 / 5824 / 5826

Slot: F1+TF1

Time: Three Hours

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

| COs | CO Statements |
|---|---|
| CO1 | To design and optimize minimal combinational circuits. |
| CO2 | To analyze and design sequential circuits utilizing various types of flip-flops. |
| CO3 | To analyze different instruction formats, addressing modes and validate efficient algorithms for fixed-point arithmetic operations. |
| CO4 | To understand the concept of memory organization and I/O fundamentals |
| CO5 | To understand the microcontroller architectural designs and parallel computing systems. |

**BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)**

**Answer ALL Questions**
**(10 X 10 = 100 Marks)**

1. Find the minimum sum-of-products and products of sum for the given expression using kmap. **CO1** **BL2**

   a) $F(a, b, c, d) = \Sigma_m(1, 2, 4, 15) + \Sigma_d(0, 3, 14)$ **[5]**

   b) $F(a, b, c, d) = \Pi_M(1, 2, 3, 4, 9, 15)$ **[5]**

2. a) Design a combinational circuit that adds one to a 4bit binary number, $A_3A_2A_1A_0$. For example, if the input of the circuit is $A_3A_2A_1A_0$=1101, the output is 1110. The circuit can be designed using four half adders. **[5]** **CO1** **BL3**

   b) A college has an automated announcement system that sends a single audio signal from the control room to one of four departments — CSE, ECE, MECH, or CIVIL — depending on a 2-bit code set by the operator.

   - The system has one input line carrying the announcement signal.
   - Two control lines $S_1$ and $S_0$ decide which department's speaker receives the signal.
   - Only one department should receive the signal at a time.

   i. Draw the logic circuit for the system using basic gates. **[2]**

   ii. Write the truth table. **[1]**

   iii. Identify the type of circuit and justify your answer. **[2]**

3. A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations: [10] CO2 BL3

$J_A = x$ $K_A = B'$

$J_B = x$ $K_B = A$

a) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables.

b) Derive the state table.

c) Draw the state diagram and logic diagram of the circuit.

4.a) I. Design an asynchronous Mod 10 counter using JK flip flops. CO2 BL3

i. Draw the state diagram and truth table. [2]

ii. Draw the logic diagram and timing diagram. [3]

II. Design a 4-bit Serial-In Serial-Out (SISO) shift register in which the complement of the last output bit (Sout) is fed back as the new serial input (Sin). Assume the initial contents of the register are 1001.

i. Draw the block diagram of the shift register. [2]

ii. Determine and tabulate the sequence of register states over the next 9 clock pulses. [3]

**OR**

4.b) Design a 3-bit synchronous up counter using D flip flop. CO2 BL3

i. Draw the State diagram and circuit excitation table. [3]

ii. Obtain simplified equation using K map. [3]

iii. Draw the logic diagram. [4]

5. a) Draw the extended structure diagram of the Von Neumann and explain the function of each block. [5] CO3 BL2

b) Express $384_{10}$ number in IEEE 32 bit and 64-bit floating-point format. [5]

6. Draw the flowchart for restoring division algorithm and perform the division for 9/3 using the same. [10] CO3 BL3

7.a) Let the address stored in the program counter be designated by the symbol X1. The instruction stored in X1 has the address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is (i) Direct (ii) Indirect (iii) PC relative (iv) Indexed? [10] CO3 BL3

OR

| | | | | |
|---|---|---|---|---|
| 7.b) | Write the program to evaluate the arithmetic expression X=(A/B)*(C+D) using 3-address, 2-address, 1-address and 0-address instructions. | [10] | CO3 | BL3 |
| 8. | Design 256 × 16 – bit RAM using 128 × 8 – bit RAM chips | | CO4 | BL3 |
| | a) What is the size of the decoder used? | [1] | | |
| | b) How many RAM chips are needed? | [1] | | |
| | c) How many address lines are required to access RAM? | [1] | | |
| | d) Design a memory-address map for the above system. | [3] | | |
| | e) Show the chip layout for the above design. | [4] | | |
| 9. | Discuss the two different data transfer modes between the central computer (CPU or Memory) and peripherals<br>a) Program-Controlled I/O<br>b) Interrupt-Initiated I/O | [10] | CO4 | BL2 |
| 10. | a) Define the concept of Instruction-Level Parallelism (ILP). | [2] | CO5 | BL2 |
| | b) Explain the different techniques used to exploit ILP such as pipelining, superscalar execution, Very Long Instruction Word (VLIW), and out-of-order execution. | [4] | | |
| | c) Discuss the major limitations and challenges of ILP. | [4] | | |

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