B/L/TY

Reg. No:

VIT
Vellore Institute of Technology

Final Assessment Test – November 2025

Course: **BEEE206L - Digital Electronics**

Class NBR(s): **1039 / 1042**

Slot: **F2+TF2**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Develop digital logic circuits and apply to solve real world applications.
CO2	Design and analyze digital circuits using Verilog HDL.
CO3	Design and implement combinational circuits, sequential circuits and programmable logic devices.
CO4	Analyze and synthesize complex digital modules and circuits for various applications.
CO5	Able to identify and prevent various hazards and timing problems in a digital design

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Use the Karnaugh map (K-map) method to minimize the Boolean function to its simplest Sum of Products (SOP) form **CO1 BL3**
   $F(A, B, C, D) = \Sigma(0, 2, 3, 6, 7) + d\ (8, 10, 11, 15)$.
   Realize the Boolean function using NAND and NOR gates.

2. Obtain the Sum of Products (SOP) form for the following Boolean expression: **CO1 BL3**
   $F(A, B, C, D) = [AB'(C + BD) + A'B']C$.
   Realize the Boolean function using NAND and NOR gates.

3. Explain how a full adder circuit can be implemented using two half adders. Draw the circuit diagram, write the logic expressions for the sum and carry outputs, and explain the working of the circuit. Write a HDL behavioural modelling code for the same. **CO2 BL3**

4. Explain the working of a 2-to-4 decoder with its truth table, boolean expressions, and a neat logic diagram. Also, discuss any two significant applications of decoder in the field of digital systems. Write a HDL Gate-Level modelling code for the same. **CO3 BL3**

5. Construct and draw the logic circuit diagram for the 2-bit magnitude comparator using universal logic gates. Write an HDL Dataflow modelling code for the same. **CO3 BL3**

4 8 9 14 15 14

8, 9, 10, 11

1, 2, 3, 6, 7, 12

6.	Explain the construction, operating principle, and timing diagram of a Master-Slave JK Flip-Flop. Discuss how this configuration resolves the race-around condition and identify its advantages and disadvantages, providing a detailed truth table and characteristic table.	CO3	BL3
7.	Draw the logic diagram to implement a D flip-flop using an JK flip-flop and explain how the inputs should be connected to achieve the toggling action. Write a HDL behavioural modelling code for the same.	CO3	BL3
8.	Design an Asynchronous Modulo-6 Counter using T Flip-Flops and Write its behavioural model code in HDL.	CO4	BL3
9.a)	Design an Asynchronous sequential logic circuit for the reduced state diagram shown in Fig.1.	CO5	BL3

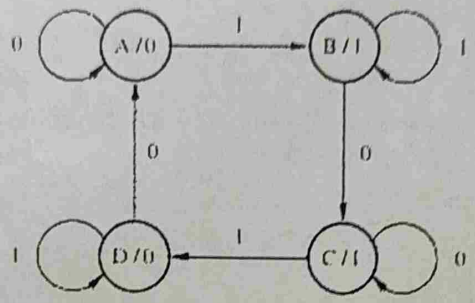

Fig.1

OR

9.b)	Explain the concept of hazards in an asynchronous sequential digital circuit. Describe the different types of hazards with suitable examples. What are essential hazards, and how can they be eliminated?	CO5	BL3
10.a)	Implement the following two Boolean functions with programmable logic array (PLA). $F_1(A,B,C) = AB' + AC + A'BC'$. $F_2(A,B,C) = (AC + BC)'$. Draw a neat circuit diagram of the PLA, clearly indicating the programmable connections in both the AND array and the OR array for the given minterms.	CO5	BL3

OR

10.b)	Explain the fundamental difference between ROM, PROM, EPROM, EEPROM, and RAM.	CO5	BL3

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