VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 24MIDO24

SLOT: E1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : M.Tech CSE [5 Year Integrated] [MIC, MID]
Course Code and Course Name : CSI1002, Operating System Principles
Faculty Name(s) : Prof. VIJAYARAJAN V, Prof. VIJAYASHERLY V, Prof. EZHIL ARASI V, Prof. MANIKANDAN G
Class Number(s) : VL2025260102450, VL2025260102453, VL2025260102456, VL2025260102458
Date of Examination : 09-10-2025
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (CO):
  CO4. Apply and analyze communication between inter process and synchronization techniques.
  CO5. Implement page replacement algorithms, memory management and to apply the file system techniques.

<table>
<tr><th>Q. No</th><th>Question</th><th>M</th><th>CO</th><th>BL</th></tr>
<tr><td>1.</td><td>Consider the processes, allocation of resources type A, B, C, D and request raised by each process as shown in above table.
<table>
<tr><th>Process</th><th>Allocation
A B C D</th><th>Request
A B C D</th><th>Available
A B C D</th></tr>
<tr><td>P0</td><td>0 1 0 2</td><td>0 0 0 0</td><td rowspan="5">1 0 1 0</td></tr>
<tr><td>P1</td><td>1 0 1 0</td><td>0 1 0 1</td></tr>
<tr><td>P2</td><td>1 1 0 1</td><td>1 0 1 0</td></tr>
<tr><td>P3</td><td>0 0 1 1</td><td>0 1 0 0</td></tr>
<tr><td>P4</td><td>0 1 1 0</td><td>1 0 0 1</td></tr>
</table>
i) Do a step-by-step execution of the Deadlock Detection algorithm. Is there a deadlock? If there is a deadlock, which processes are involved? [6 Marks]
ii) If a request from process P1 for two more instances of type D arises, then explain the context of the resulting system. Provide your conclusions appropriately. [4 Marks]</td><td>10</td><td>CO4</td><td>BL3</td></tr>
<tr><td rowspan="2">2.</td><td>a) Suppose that in a system of five processes and five resources, the following describes the snapshot of the system.
Assignment Edges: R1→P1, R2→P2, R3→P3, R4→P4, R5→P5
Request Edges: P1→R4, P2→R1, P2→R3, P3→R5, P4→R2, P5→R4.
Total Resources configured: [2,3,1,1,3]
i) Draw the Resource Allocation Graph (RAG)
ii)Convert the RAG into the matrix representation (i.e., Allocation, Request and Available)
iii) List the cycle(s) and provide your interpretations.</td><td>5</td><td>CO5</td><td>BL3</td></tr>
<tr><td>b) Consider five programs (in order) with their size (in KB): P0 = 602, P1 = 14, P2= 100, P3 =580, and P4 = 95. Assume at that time, the available free space partitions of memory (in order) are 1200–1805, 50 – 160, 220-234, and 2500-3180. Draw the memory layouts upon allocating to these processes using First-fit, Worst-fit and Best fit memory allocation strategies. Compare their performance.</td><td>5</td><td></td><td></td></tr>
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3.	Two processes P0 and P1 are using Peterson's algorithm to access a shared resource. The variables are initialized as:
	flag[0] = false; flag[1] = false; turn = 0;
	Let us now assume the following sequence of events:
	1. P0 executes:
	flag[0] = true; turn = 1;
	2. Before P0 enters its while-loop, P1 executes:
	flag[1] = true; turn = 0;
	3. Both processes now reach their while (flag[j] && turn == j); condition simultaneously.
	a) In this situation, which process will be allowed to enter the critical section first and why?
	b) What would happen if the turn variable assignment was removed from the algorithm, would the mutual exclusion property still hold in this scenario? Explain.
	c) If both processes continuously try to enter their critical sections back-to-back (no remainder section), explain how Peterson's algorithm prevents starvation in this case.
		10	CO4	BL4

4.	a) Let m[0]...m[7] be mutexes (binary semaphores) and P[0] .... P[7] be processes. Suppose each process P[i] executes the following at the same time then what would be the state of the system of 7 processes: wait (m[i]);wait (m[(i+1) mod 7]); ..... signal (m[i]); signal (m[(i+1) mod 7]); Justify your answer appropriately and provide solutions for the cause thus identified.	5	CO4	BL4
	b) Assume that there are three students in a Chemistry laboratory. A student must have three components to perform an experiment: pipette, burette and a conical flask. Each student is having a different item (and only one) of the three required items. A supervisor being the fourth person in the laboratory, has unlimited capacity of all these items. If no student is experimenting, the supervisor places two of the three items (chosen at random) onto a lab table. The student who is ready to perform the experiment can pick the two items (if appropriate) and start performing the experiment. When done with the experiment, the student notifies the supervisor and the process will repeat. Provide a solution to synchronize the activities as mentioned. Design the synchronization problem stated above through a pseudocode.	5		
5.	a) Consider the following segment table: What are the physical addresses of each of the following logical addresses? (i) 1, 200 (ii) 4, 423 (iii) 2, 368 (iv) 3, 895 (v) 0, 499 [3 Marks]	10	CO5	BL3
	b) Consider a paging system with the page table stored in memory. i) If a memory reference takes 300 nanoseconds, how long does a paged memory reference take? ii) If we add associative registers, and 65 percent of all page-table references are found in the associative registers, what is the effective memory reference time? (Assume that finding a page-table entry in the associative registers takes zero time, if the entry is there) [4 marks]			
	c) In a 2-level paging scheme, let the page size be 32 KB, logical addresses be 39 bits, physical memory be 32 MB and page table entry size be 8 bytes. How does a logical address split into 3 parts namely outer page, inner page, and offset (denoted as p1, p2, offset)? [3 marks]			

Segment	Base	Length
0	2400	500
1	3011	250
2	5021	369
3	7506	895
4	6200	423

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