Reg. No: 23BML0045

Z/K/TY

Final Assessment Test – November 2025

VIT Vellore Institute of Technology

Course: BECE303L - VLSI System Design

Slot: D2+TD2

Class NBR(s): 0388 / 0390 / 0392 / 0394

Max. Marks: 100

Time: Three Hours

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	Analyze the CMOS digital electronics circuits, including logic components and their interconnect using mathematical methods and circuit analysis models
CO2	Create models of moderately sized CMOS inverters with specified noise margin and propagation delay.
CO3	Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnects.
CO4	Analyse the various logic families and efficient techniques at circuit level for improving power and speed of combinational and sequential logic.
CO5	Implement the CMOS digital circuits with the specified timing constraints.
CO6	Design memories with efficient architectures to improve access times, power consumption

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Using the measured data given below, determine the device parameters V_{T0}, k, γ, and λ, assuming $2\phi_F = -0.6$ V **CO1 BL3**

V_{gs}	V_{ds}	V_{bs}	I_D [uA]
2	5	0	10
5	5	0	400
5	5	-3	280
5	8	0	480

2. (a) A PMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 10^{16}$ cm^{-3}, gate doping density (n-type poly) of $N_D = 10^{20}$ cm^{-3}, $Q_{ox}/q = 4 \times 10^{10}$ cm^{-2} and gate oxide thickness of $t_{ox} = 0.1\ \mu m$. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. Use $\varepsilon_{si} = 11.7\varepsilon_0$. **[6] CO1 BL3**

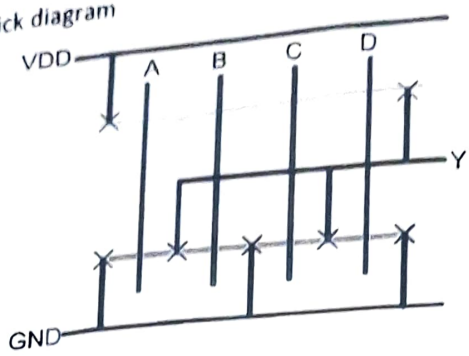
(b) Consider a diffusion area that has the dimensions $10\ \mu m \times 5\ \mu m$ and the abrupt junction depth is $0.5\ \mu m$. Its n-type impurity doping level is $N_D = 1 \times 10^{20}$ cm^{-3}and the surrounding p-type substrate doping level is $N_A = 1 \times 10^{16}$ cm^{-3}. Determine the capacitance when the diffusion area is biased at 5 V and the substrate is biased at 0 V. In this problem, assume that there is no channel-stop implant. **[4]**

3. Derive the expression of the output voltage of the CMOS inverter for Region-D of the voltage transfer curve. **CO2 BL2**

Minimize the Boolean function and implement it as a single-stage static CMOS gate. CO2 BL3

$F(w,x,y,z) = \Sigma\,(0, 1, 4, 7, 8, 11, 13)$ CO3 BL3

5.(a) For the given Stick diagram



a) For 20 nm CMOS Technology, $\lambda = 10\ nm$, so the minimum feature size equals 2λ. Estimate the Area from the stick diagram.

b) Draw the static CMOS schematic for the given Stick Diagram with proper transistor sizing. Assume :

(i) The resistance of the NMOS transistor with unit width is R

(ii) The resistance of the PMOS transistor with unit width is 3R

The circuit should be designed such that the pull-up and pull-down path resistances of the implemented logic gate are equal to those of a unit-sized CMOS inverter.

OR

5.(b) Consider the design of a CMOS compound OR-OR-AND-INVERT (OAI22) gate computing **CO3 BL3**

$$Y = \overline{A(D+E).(BC)}$$

(i) Sketch a transistor-level schematic

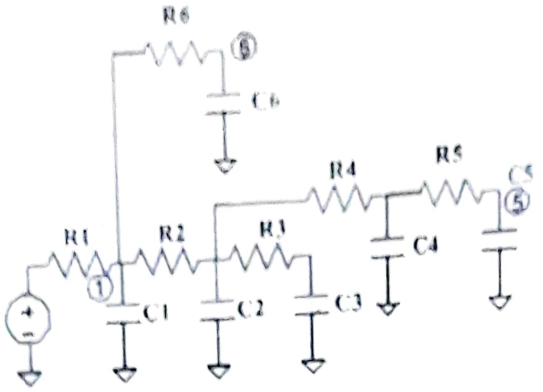
(ii) Sketch a stick diagram

(iii) Estimate the area from the stick diagram if the technology node is 90nm.

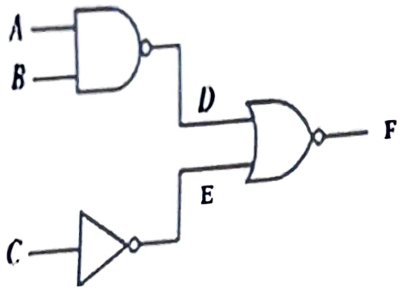
6. a) The RC network in the figure models a CMOS interconnect driven by a logic gate. all resistors have a value of R=2 Ω, and all capacitors have a value of C=5 fF. Using the Elmore delay model, calculate the propagation delay at the following nodes: **[5] CO4 BL3**

i. Node 1

ii. Node 5



b) Let CL = 50 fF for each signal output node, VDD = 2.0 V, and f_{Clk} = 1.5 GHz. Create a truth table for the circuit and calculate the expected power dissipation for the $0 \rightarrow 1$ transition. [5]



[5] CO4 BL3

a) Draw the static CMOS circuit for

$$Y = \overline{(DE) + A(B + C)}$$

with pull-up/pull-down resistances matched to a unit inverter.

Compute (i) the logical effort of each input, (ii) the electrical effort assuming an FO4 load ($C_L = 4C_{inv}$), and (iii) parasitic delay. [5]

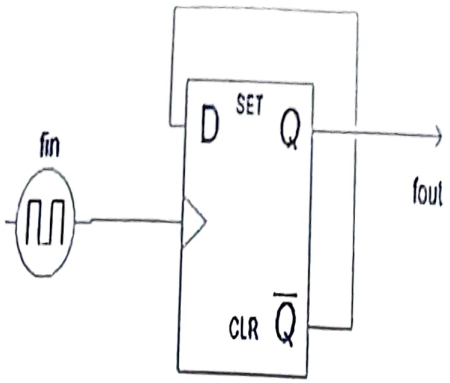
b) Consider three alternative circuits for driving a load 50 times the input capacitance of the circuit. The first design utilizes one inverter, the second employs three inverters in series, and the third utilizes five inverters in series. All three designs compute the same logic function. Which is best, and what is the minimum delay?

CO5 BL3

The setup time of the flip-flop is 6 ns, the hold time is 2 ns, and the clock-to-Q delay is given as 10 ns.

a) Calculate the minimum clock period and maximum clock frequency required to handle the circuit.

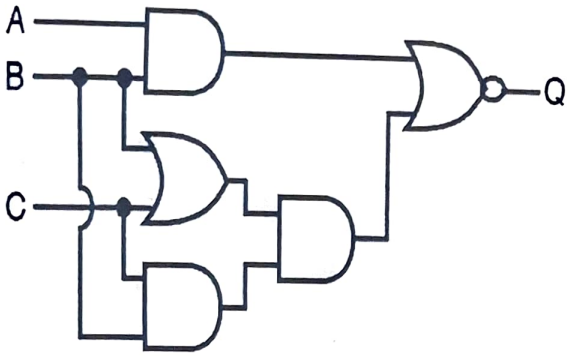
b) Also, determine the setup and hold time violations if any and give a proper reason in case of violation.



9.(a) Design the given circuit using the following circuit family: **CO4 BL3**

i) Pass Transistor Logic

ii) Pseudo-NMOS Logic



OR

9.(b) Implement the given function using transmission gate logic. **CO4 BL3**

$F(w, x, y, z) = \Sigma (1,2,3,5,6,7,8,12,13)$

10. *With a neat diagram, explain the structure and working of a 1T1C DRAM cell. Describe in detail the write, read, and refresh operations. Also, explain why DRAM is preferred over SRAM for main memory applications.* **CO6 BL2**

⇔⇔⇔ **Z/K/TY**⇔⇔⇔