REG.NO.:

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

NAME OF THE SCHOOL
CONTINUOUS ASSESSMENT TEST - II
XXX SEMESTER 2025-2026

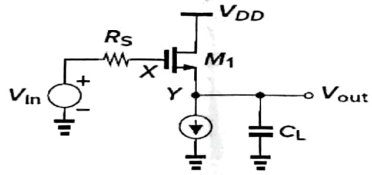
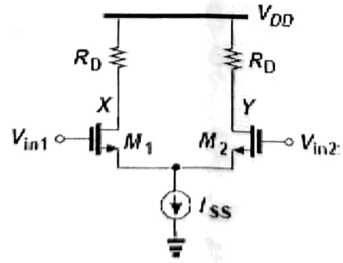
SLOT: A2+TA2

Programme Name & Branch : **B.Tech - Electronics Engineering (VLSI Design and Technology)**

Course Code and Course Name : **BEVD304L - CMOS Analog IC Design**
Faculty Name(s) : **Dr Abdul Majeed K K**
Class Number(s) : **VL2025260500917**
Date of Examination : **15/03/26**
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  2. Design single-stage, differential amplifiers, and analyse the performance with respect to frequency and noise
  6. Understand the fundamentals of PLL

Q. No	Question	M
1.	Consider the source follower shown in Fig. 1 where all the transistors have $(W/L)_{M1}$ = 100 µm/1 µm; $\mu_n C_{ox}$ = 90 µA/V^2; $\mu_p C_{ox}$ = 30 µA/V^2; I_{bias} = 100 µA; γ = 0.5 V$^{1/2}$; $2\emptyset_F$ = 0.8 V; V_{SB} = 0.4 V; R_S = 180 kΩ; C_L = 10 pF; C_{GS1} = 0.2 pF; C_{GD1} = 15 fF; C_{SB1} = 40 fF. Determine the low frequency gain Av and estimate the poles and zero frequency.  Fig. 1	10
2.	Consider a MOSFET differential amplifier in Fig. 2 operated at a bias current of 0.5 mA, using transistors with a (W/L) of 5 µm/1 µm, $\mu_n C_{ox}$ = 0.3 mA/V^2, R_D = 8 kΩ and R_{SS} = 8 kΩ, CL = 1 pF, C_{GS} = 30 fF, C_{GD} = 15 fF and C_{DB} = 15 fF, $\lambda_n = \lambda_p$ = 0.1 V^{-1}. Estimate the pole and Zero frequencies.  Fig. 2	10

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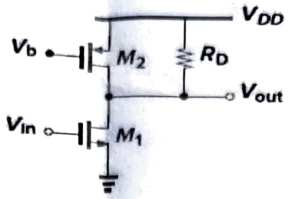
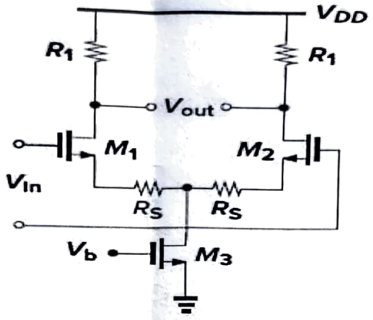
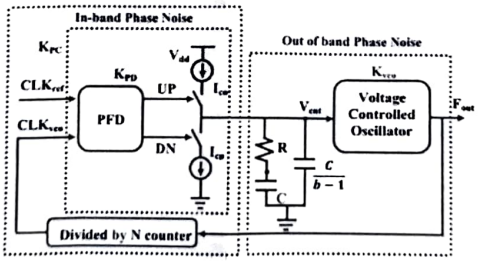
3.	Determine the input referred noise of CMOS inverter shown in Fig. 3 for $\lambda \neq 0$. Consider both thermal and flicker noises.  Fig. 3	5
4.	Derive the input referred thermal noise of the opamp shown in Fig. 4.  Fig. 4	5
5.	The PLL architecture is given in Fig.5. Calculate its open 1) loop transfer function, 2) closed loop transfer function, 3) natural frequency (ωn), 4) Damping factor (ζ), 5) Output frequency (Fout) and 6) locking time for 1% tolerance. The values of PLL components are as follows Fref=18 MHz, N=128, C= 260 ps, b= 10, R= 1 KΩ, Icp= 150μA, Kvco= 19 GradV^{-1}.  Fig. 5	10

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