U/D/TZ

Reg. No: 24BCI0069

VIT
Vellore Institute of Technology

Final Assessment Test – April 2026

Course: BCSE205L - Computer Architecture and Organization

Class NBR(s): 1866/1870/1874/1875/1880/1896/1898/1901/1903/1953/1968/1974/1976/1985/1988/1998/2001/2006/2022/2024/2028/2231/3865/3879/4005/5391

Slot: A1+TA1

Time: Three Hours

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating-point arithmetic operations.
CO2	Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction
CO3	Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
CO4	Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Consider a user is accessible with eight registers of the give CPU. Draw the design to select the specific register for reading or writing operation. **CO1 BL3**

List the various registers of IAS machine.

Mention the condition code that has influence on register.

2. a) Perform the 2's complement addition for the value "c2"-"3f", indicate what are the flags that are affected. **CO1 BL3**

b) What are the various codes that are used for information interchange (transition from 4bit to 16 bit). Out of it, which was the recent one used in the market for web development?

c) Discuss the various floating point number representation of normal and IEEE.

3. Assume c=a+b, write the two address instruction to perform the above operation. Consider a, b are stored in some memory location. Identify the total instruction cycle. List the phases of the instruction for any instruction written with the description of each. **CO1 BL4**

4. Consider the following instruction mix **CO1 BL2**

Operation	frequency	cycle count	weighted CPI_i
ALU ops	50%	1	_____
Loads	20%	2	_____
Stores	10%	3	_____
Branches	20%	4	_____

a) What is the average CPI? (Use the weighted arithmetic average.)
b) What is the cycle count distribution according to operation type?
c) What will be the overall performance of the system while executing these instructions?
d) If branch cycles are reduced to 2, do you have enough information to determine how much faster the modified processor will be than the original processor?

5. Consider a 4-way set associative cache memory with total 8 cache lines and a main memory with 256 blocks. Find the memory blocks which will be present in the cache after the following sequence of memory block references with the following block replacement algorithms. Assuming that initially the cache is empty.0 2 7 8 4 3 6 2 13 22 28 53 7 27 53 18 55 11 82 **CO2 BL3**

A) LRU policy is used for cache block replacement.
B) FIFO policy is used for cache block replacement.

Calculate the cache hit and miss. Identify which policy will be better for block data given.

6. What is the various possible design for RAM and ROM with larger memories? Differentiate the memory address calculation and how does it enhance in reducing the time duration. **CO2 BL4**

Draw the design to access a larger memory capacity of 512 X 16 RAM and 1024X16 ROM with an available capacity of 128X16 and 256X16 RAM and ROM respectively. Use only one decoder for both RAM and ROM. Mention all the necessary signal required for memory access.

7. a) Differentiate programmed IO, interrupt driven IO and DMA considering the key feature. Provide a suitable example for each of it. **CO3 BL2**
b) What is primary role of bus arbitration in computer systems? Identify the different types of bus arbitration, explain with a suitable example considering clock.

8. A data sequence of 101101001001 is transmitted using an error correction mechanism. During transmission, bit at the 6^{th} position is altered (i.e, a 0 changes to 1 or a 1 changes to 0). CO4 BL3

a) Explain how the data sequence at the transmitter side is enabled for error correction reference.

b) Show the steps involved in erroneous bit identification in the receiver side.

c) Depict both the sender and receiver side error correction mechanism.

9.a) Perform booth recoding multiplication, provide the steps as assumed in the form of A, Q, Q-1 register. Consider the values -13X-21 with 8 bits of manipulation. Draw the flowchart illustrating the manipulation. CO1 BL4

OR

9.b) Perform restoring division for 15/4. Provide the steps as assumed in the form of A, Q, register. Draw the flowchart illustrating the manipulation. CO1 BL4

10.a) Explain the concept of pipeline Hazard? Discuss the different type of hazards with suitable example. CO4 BL3

OR

10.b) Discuss about each with suitable diagram if applicable CO4 BL3

i. Scalar architecture
ii. Super scalar
iii. Pipeline
iv. Superscalar pipeline
v. Role of Amdahl's law in pipeline processor.

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