REG.NO.: [redacted]

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-26

SLOT: D2+TD2

Programme Name & Branch	: BVD
Course Code and Course Name	: BEVD207L and Computer Architecture
Faculty Name(s)	: Dr. Vikas Vijayvargiya
Class Number(s)	: VL2025260500890
Date of Examination	: 30-Jan-2026
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes
  CO1: Understand the basic structure of computers, operations, and instructions
  CO2: Understand the Arithmetic and Logic Unit (ALU) and the implementation of fixed-point and floating-point arithmetic units.
  CO4: Understand the processor design and control unit.

<table>
<tr><th>Q. No</th><th>Question</th><th>M</th><th>CO</th><th>BL</th></tr>
<tr><td>1.</td><td>Discuss the Von-Neumann architecture of a computer with a suitable example. Also explain its limitations and discuss other possible computer architectures.</td><td>10</td><td>1</td><td>2</td></tr>
<tr><td>2.</td><td>Programs P1 and P2 are executed on two machines M1 and M2. The execution times are shown below.
<table>
<tr><th>Program</th><th>M1 (s)</th><th>M2 (s)</th></tr>
<tr><td>P1</td><td>8</td><td>12</td></tr>
<tr><td>P2</td><td>3</td><td>6</td></tr>
</table>
I. For each program, identify the faster machine and calculate the relative speedup.
II. Program P1 executes 400 million instructions on M1 and 240 million instructions on M2. Determine the instruction execution rate on both machines.
III. If the clock rates of M1 and M2 are 250 MHz and 500 MHz, respectively, calculate the CPI for program P1 on each machine</td><td>10</td><td>1</td><td>3</td></tr>
<tr><td>3.</td><td>Using 5-bit 2's complement representation, perform the signed multiplication using Booth's algorithm: (−7) × (+5). Draw the Booth multiplier Datapath and briefly explain how the Control Unit controls the Datapath to execute the multiplication instruction.</td><td>10</td><td>2</td><td>3</td></tr>
<tr><td>4.</td><td>Explain IEEE-754 single-precision floating-point multiplication with the help of a neat FPU block diagram, briefly describing the function of each hardware block. Then, perform the floating-point multiplication of 2.75×1.5 using IEEE-754 single-precision format.</td><td>10</td><td>2</td><td>3</td></tr>
</table>

REG.NO.:

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-26

SLOT: D2+TD2

5.	A processor has 32 general-purpose registers and a fixed instruction length of 16 bits. The main memory size is 256 bytes. The instruction set consists of: • 32 Type-I instructions, each having two register operands • 2 Type-II instructions, each having one register operand and one memory operand • N Type-III instructions, each having one register operand a) Find the maximum possible value of N. b) Draw suitable instruction formats for all three instruction types. c) Explain how the processor distinguishes between different instructions formats.	10	4	4