REG.NO.:

# VIT®

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

SLOT: A1+TA1

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|---|---|
| **Programme Name & Branch** | **: B. Tech (EEE & EI)** |
| **Course Code and Course Name** | **: BAEEE201, Digital Electronics** |
| **Faculty Name(s)** | **: Dr. Dhanamjayulu C, Dr. Rajesh Kumar Lenka** |
| **Class Number(s)** | **: VL2025260504310, VL2025260504311** |
| **Date of Examination** | **:27/01/2026** |
| **Exam Duration** | **: 90 minutes** **Maximum Marks: 50** |

**General instruction(s):**

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (**Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)**

  CO1. To understand the fundamental concepts of digital logic components and circuits.
  CO2. To construct the combinational and sequential logic circuits for different applications.
  CO3. To implement digital circuits in programmable logic devices.

| Q. No | Question | M | CO | BL |
|---|---|---|---|---|
| 1. | An on-board electric vehicle (EV) charger uses digital protection signals: A-Input over-voltage detected, B-Charger over-temperature detected, C-Output over-current detected, D-Grid fault/isolation fault detected to decide whether the charger should shut down or not, depending upon the following operating conditions.<br>**Condition-1:** The charger must shut down immediately if a grid/isolation fault occurs, OR any two or more of the faults (A, B, C) occur simultaneously.<br>**Condition-2:** The charger continues operation if: Only one of (A, B, C) is active and D is inactive.<br>However, the digital protection system is subjected to two constraints: 1- Input overvoltage and output overcurrent never occur together, 2- Grid fault is never detected when all other signals are healthy. Design the EV charger digital protection system by using universal logic gates. | 10 | 1 | 4 |
| 2. | A digital measurement and control unit receives data from a rotary position sensor to minimize transition errors during mechanical movement. The encoder internally uses a reflected Gray code to minimize switching errors, while the digital controller operates using BCD-encoded sector numbers for diagnostics and fault logging. To interface these two subsystems, design a custom code-conversion block by using logic gates. | 10 | 2 | 3 |
| 3. | Draw a NAND logic diagram that implements the complement of the following function after minimization:<br>$F(A, B, C, D) = \sum m(1, 2, 3, 6, 10, 11, 14)$ | 10 | 1 | 3 |
| 4. | Design a combinational circuit with three inputs, *X*, *Y*, and *Z*, and three outputs, *A*, *B*, and *C*. When the binary equivalent input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary equivalent input is 4, 5, 6, or 7, the binary output is two less than the input. | 10 | 2 | 3 |
| 5. | Implement a half-subtractor and a full subtractor by using a 4:1 multiplexer. | 10 | 2 | 3 |

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