V/D/TZ

Reg. No: 24BCE0366

Final Assessment Test – April 2026

VIT® Vellore Institute of Technology (Deemed to be University under section 3 of the UGC Act 1956)

Course: **BCSE205L - Computer Architecture and Organization**

Class NBR(s): **1867/1868/1872/1873/1878/1883/1885/ 1899/1902/1956/1958/1960/1965/1969/1975/1978/ 1987/1989/1991/1996/2003/2023/2026/6059**

Slot: **A2+TA2**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.
CO2	Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
CO3	Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
CO4	Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1.	Discuss the organization of the IAS computer architecture with neat sketch and analyze how an instruction is executed in this system, highlighting the role of registers such as PC, MAR, MBR, IR, IBR, AC, and MQ, and the instruction fetch and execution sequence with a suitable example.		CO1	BL2
2.	Perform division using the Restoring division algorithm for the following: Dividend =29, Divisor = 5. Show the contents of A, Q, and M registers for each step and draw the flow chart.		CO1	BL3
3.a)	I. Perform multiplication of –15 and 13 using Booth's algorithm. Show the contents of AC, QR, and Q_{n+1} in each step with a neat flowchart.	[7]	CO1	BL3
	II. Represent the decimal number –13.625 in IEEE 754 single-precision and double precision floating point format.	[3]		
	OR			
3.b)	Analyze the algorithm used for floating-point addition and subtraction operations, and design a flowchart that clearly represents the sequence of steps involved in the floating-point addition and subtraction process.		CO1	BL4

4. a) Consider the following values: [5] CO1 BL3

- Address field of instruction = 300
- Register R1 = 100
- Memory location 300 contains 700
- Memory location 700 contains 900

Determine the effective address for the following addressing modes:
Direct, Indirect, Register Indirect, and Indexed addressing modes.

b) Analyze the phases of the instruction cycle and describe the sequence of micro-operations performed in each phase during instruction execution. [5] CO1 BL4

5. Explain in detail and compare Hardwired Control and Micro-programmed Control units in computer systems. Discuss their differences in terms of speed, flexibility, complexity, and applications. Support your answer with a neat diagram. CO1 BL3

6. a) A set-associative cache memory contains 128 cache blocks, which are organized into sets of 4 blocks each. The main memory consists of 16,384 blocks, and each block contains 256 words, where each word is 8 bits. Determine the total number of bits required to address the main memory. Analyze the number of bits required for the TAG, SET, and WORD (offset) fields in the memory address. [5] CO2 BL3

b) A cache memory can hold 4 blocks. The processor generates the following sequence of memory block references: [5]

1, 2, 3, 4, 2, 1, 5, 2, 4, 5, 3, 2

Simulate the FIFO (First-In-First-Out) and LRU replacement policy for the following.

- Show the cache contents after each reference in a table.
- Identify cache hits and cache misses.
- Calculate the total number of misses and hits.
- Calculate the hit ratio and Miss ratio.

7. a) A computer system employs a write-back cache with a 80% hit ratio for writes. The cache operates in "Look Aside" and has a 90% read hit ratio. Reads account for 65% of all memory references and writes account for 35%.If the main memory cycle time is 250ns and the cache access time is 35ns, what would be the average access time for all references (reads as well as writes)? [4] CO2 BL3

b) A computer system is to be designed with 512 × 8 RAM and 256 × 8 ROM using available 256 × 8 RAM and 128 × 8 ROM memory chips. Determine the number of chips required by constructing the memory requirement table, develop the memory address map, and illustrate the overall memory organization with a neat chip layout diagram. [6] CO2 BL6

8. a) In computer systems, large amounts of data often need to be transferred between memory and I/O devices efficiently. Continuous involvement of the CPU in such transfers can slow down overall system performance. [5] CO3 BL2

- Explain how communication between memory and I/O devices is made possible without constant CPU intervention.
- Describe the architecture and working of the controller used for this communication, with the help of a neat diagram.

b) In a university computer lab, several devices such as a printer, a scanner, and a projector are connected to the system one after another in a specific order. When the projector sends a request to access the controller, it cannot be serviced immediately because the printer and scanner requests must be checked first in the order they are connected. Identify the technique used here to handle multiple requests. Justify your answer with a neat diagram. [5] CO3 BL3

9.a) Compare RAID levels 0, 1, 5, and 6 in terms of performance, fault tolerance, storage efficiency, and minimum disk requirements. Illustrate your answer with neat diagrams. Which RAID level would you recommend for mission-critical applications and why? CO4 BL5

OR

9.b) I. Explain the principle of Hamming code and how it enables single-bit error detection and correction. [5] CO4 BL2

II. For the 8-bit data word 10110101, use the Hamming algorithm to find how many check bits are needed, place them in the correct positions, calculate their values, and write down the final encoded word. Show your working clearly and illustrate your answer with a neat diagram of bit positions. [5] CO4 BL3

10. a) A parallel processor is designed to accelerate 75% of a program using 8 processors. Remaining 25% is sequential. [5] CO4 BL3

i. Calculate the theoretical speed-up using Amdahl's Law.
ii. Compute efficiency of the parallel system.
iii. If processors are increased to 16, calculate new speed-up.
iv. Comment on the scalability of the system.

b) Consider the following instructions executed in a 5-stage pipeline. [5]

I1: LOAD R1, 10(R2)
I2: ADD R3, R1, R4
I3: MUL R5, R3, R6
I4: SUB R7, R5, R8
I5: STORE R7, 4(R2)

Identify the hazards present. Explain why they occur. Suggest methods to resolve them. Mention one drawback of each method.

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