Course Code	Course Title	L	T	P	C
BAEVD301	Verification Methodologies	3	0	2	4
Pre-requisite	BAEVD102 Digital System Design	Syllabus Version			
		1			

Course Objectives

1. Understand the concepts of VLSI Verification Methodologies
2. Develop skills in writing testbenches using System Verilog
3. Apply industry standard framework for Verification

Course Outcomes

1. Interpret the basic test environment for verification
2. Implement system Verilog test environment
3. Implement reusable class based test environment
4. Interpret coverage metrics and improve verification efficiency
5. Employ industry-standard framework for verification

Module:1	Fundamentals of Verification	9 hours

Introduction to VLSI verification - Types of verification - Functional Verification challenges and solutions – Functional Verification Process - Verification planning – Basic Testbench Functionality – Layered Testbench - Directed Testing – Constrained Random Stimulus – Coverage – Code Coverage and Functional Coverage

Module:2	System Verilog	9 hours

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – Packages – operators – expressions – Procedural statements and control flow – Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine – SV scheduling semantics – Developing System Verilog Test environment – Case Study

Module:3	OOP based Testbench	8 hours

OOP Terminology - Creating Object - object deallocation - copying objects - static variables - Global variables – Inheritance – Polymorphism – Program – Interface - Stimulus timing - Module interactions (Mailbox, Semaphores) - Connecting together – Developing reusable object based self-checking test environment – Generator – Transactor – Driver - Monitor – Scoreboard – Case Study

Module:4	Randomization, Functional Coverage	8 hours

Need for Randomization – Randomization in System Verilog – Constraint Details – Solution Probabilities – Controlling Multiple Constraint Blocks – Valid Constraints – In-line Constraints – Common Randomization Problems - Coverage Types – Anatomy of covergroup – Triggering a covergroup – Data Sampling – Cross

Coverage – Coverage options – Developing constraint random verification environment		
Module:5	**Universal Verification Methodology (UVM) Basics**	**9 hours**
System Verilog test environment Vs UVM based test environment - Basics of UVM Transaction Level Communication Protocol - Developing reusable verification components - Developing reusable verification environment – Case Study		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

Ashok B. Mehta, "**Introduction to System Verilog**", Springer, New York, 1st Edition, **2021**
Srivatsa Vasudevan, "**Practical UVM Step by Step with IEEE 1800.2**", R R Bowker, CA, USA, 2nd Edition, **2020**

Reference Books

Ashok B. Mehta, "**ASIC/SoC Functional Design Verification – A Comprehensive guide to Technologies and Methodologies**", Springer, New York, 1st Edition, **2017**
Christian B Spear, "**System Verilog for Verification: A guide to learning the Testbench language features**", Springer, 3rd Edition, **2012**

Indicative Experiments

1. Developing self-checking Verification Environment in Verilog	2 hours
2. Arrays in System Verilog	2 hours
3. Inheritance & Polymorphism	2 hours
4. Mailbox	2 hours
5. Developing reusable verification components	4 hours
6. Class based System Verilog self-checking test environment for FIFO	4 hours
7. Coverage	2 hours
8. UVM test environment	2 hours
9. UVM Components	4 hours
10. UVM testbench for APB/AHB Protocol	6 hours
Total Laboratory Hours:	**30 hours**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025