Course code	Course Title	L	T	P	C
BITE301L	Computer Architecture and Organization	3	0	0	3
Pre-requisite	BITE202L, BITE202P	Syllabus version			
		1.0			

Course Objectives:

1. To familiarize students with the basic structure of computer systems and impart knowledge on performance measurement, instruction sequencing I/O organization and interfacing techniques.
2. To impart knowledge of data representation and implementation of arithmetic operations using algorithms.
3. To acquaint the importance of memory systems, their performance metrics and to customize the hardware to improve system performance.

Course Outcomes:

1. Elucidate the arithmetic operations, addressing modes and the performance of computers.
2. Design instruction level parallelism using instruction stages. Understand pipelining concepts and identify the hazards to rectify in typical processer pipeline.
3. Analyse the arithmetic algorithms to perform ALU operations.
4. Design a memory system on understanding the chip organization and analyse its performance.
5. Understand the concepts of Parallel processing, Multiprocessors and Multicomputer.

Module:1	Basic Structure of Computers	5 hours

Computer Types - Functional Units - Basic Operational Concepts - Bus Structures - Performance - Processor, Clock, Performance Equation - Pipelining and Superscalar Operation - Clock Rate - Instruction Set: CISC and RISC, Compiler, Performance Measurement, Multiprocessors and Multicomputer - Historical Perspective

Module:2	Machine Instructions and Programs	7 hours

Numbers - Arithmetic Operations and Characters - Memory Locations and Addresses - Memory Operations - Instructions and Instruction Sequencing - Addressing Modes - Assembly Language - Basic Input/Output Operations - Stacks and Queues - Subroutines - Encoding of Machine Instructions

Module:3	Input/Output Organization	5 hours

Accessing I/O Devices – Interrupts - Processor Examples - Direct Memory Access – Buses - Interface Circuits - Standard I/O Interfaces

Module:4	Memory System	7 hours

Semiconductor RAM Memories - Read-Only Memories – Speed - Size and Cost -Cache Memories - Performance Consideration - Virtual Memories - Memory Management Requirements - Secondary Storage.

Module:5	Arithmetic	7 hours

Addition and Subtraction of Signed Numbers - Multiplication of Positive Numbers - Signed-Operand Multiplication - Integer Division - Floating Point Numbers and Operations

Module:6	Pipelining	7 hours

Basic Concepts - Data Hazards - Instruction Hazards - Influence on Instruction Sets - Data Path and Control Considerations - Performance Considerations

Module:7	Large Computer Systems	5 hours

Forms of Parallel Processing - Array Processors - Structure of General Purpose Multiprocessors - Interconnection Networks - Memory Organization in Multiprocessors -

Program Parallelism and Shared variables – Multicomputer - Performance Considerations			
Module:8	**Contemporary Issues**		**2 hours**
	Total Lecture hours:		**45 hours**
Text Book			
1.	Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", 2017(Reprint of 2011), 5th Edition, Tata Mc-Graw Hill.		
Reference Books			
1.	Patterson, D. A., and J. L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 2016, 5th Edition, Morgan Kaufman.		
2.	Hayes, J.P., "Computer Architecture and Organization", 2017, 5th Edition, Tata Mc-Graw Hill.		
3.	William Stallings "Computer Organization and architecture- Designing for Performance", 2019, 11th Edition, Prentice Hall.		
Mode of Evaluation: Continuous Assessment Tests, Assignment, Quiz, Final Assessment Test			
Recommended by Board of Studies	20-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022